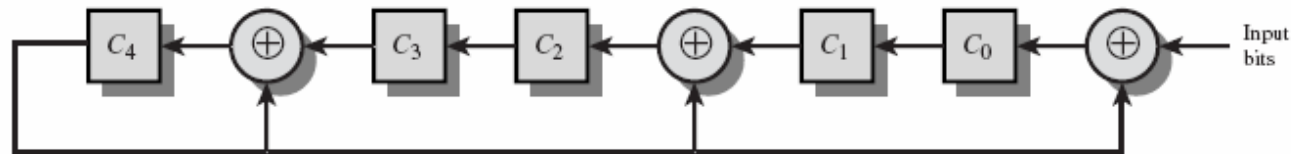


# CRC Generator and Example: from Stallings "Data & Comp. Commun."



□ = 1-bit shift register    ⊕ = Exclusive-OR circuit

(a) Shift-register implementation

|         | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | $C_4 \oplus C_3$ | $C_4 \oplus C_1$ | $C_4 \oplus \text{input}$ | input |                      |
|---------|-------|-------|-------|-------|-------|------------------|------------------|---------------------------|-------|----------------------|
| Initial | 0     | 0     | 0     | 0     | 0     | 0                | 0                | 1                         | 1     | } Message to be sent |
| Step1   | 0     | 0     | 0     | 0     | 1     | 0                | 0                | 0                         | 0     |                      |
| Step2   | 0     | 0     | 0     | 1     | 0     | 0                | 1                | 1                         | 1     |                      |
| Step3   | 0     | 0     | 1     | 0     | 1     | 0                | 0                | 0                         | 0     |                      |
| Step4   | 0     | 1     | 0     | 1     | 0     | 1                | 1                | 0                         | 0     |                      |
| Step5   | 1     | 0     | 1     | 0     | 0     | 1                | 1                | 1                         | 0     |                      |
| Step6   | 1     | 1     | 1     | 0     | 1     | 0                | 1                | 0                         | 1     |                      |
| Step7   | 0     | 1     | 1     | 1     | 0     | 1                | 1                | 1                         | 1     |                      |
| Step8   | 1     | 1     | 1     | 0     | 1     | 0                | 1                | 1                         | 0     |                      |
| Step9   | 0     | 1     | 1     | 1     | 1     | 1                | 1                | 1                         | 1     |                      |
| Step10  | 1     | 1     | 1     | 1     | 1     | 0                | 0                | 1                         | 0     | } Five zeros added   |
| Step11  | 0     | 1     | 0     | 1     | 1     | 1                | 1                | 0                         | 0     |                      |
| Step12  | 1     | 0     | 1     | 1     | 0     | 1                | 0                | 1                         | 0     |                      |
| Step13  | 1     | 1     | 0     | 0     | 1     | 0                | 1                | 1                         | 0     |                      |
| Step14  | 0     | 0     | 1     | 1     | 1     | 0                | 1                | 0                         | 0     |                      |
| Step15  | 0     | 1     | 1     | 1     | 0     | 1                | 1                | 0                         | —     |                      |

(b) Example with input of 1010001101

Figure 7.6 Circuit with Shift Registers for Dividing by the Polynomial  $X^5 + X^4 + X^2 + 1$

# Ring Network Interface: from Stallings "Data & Comp. Commun."

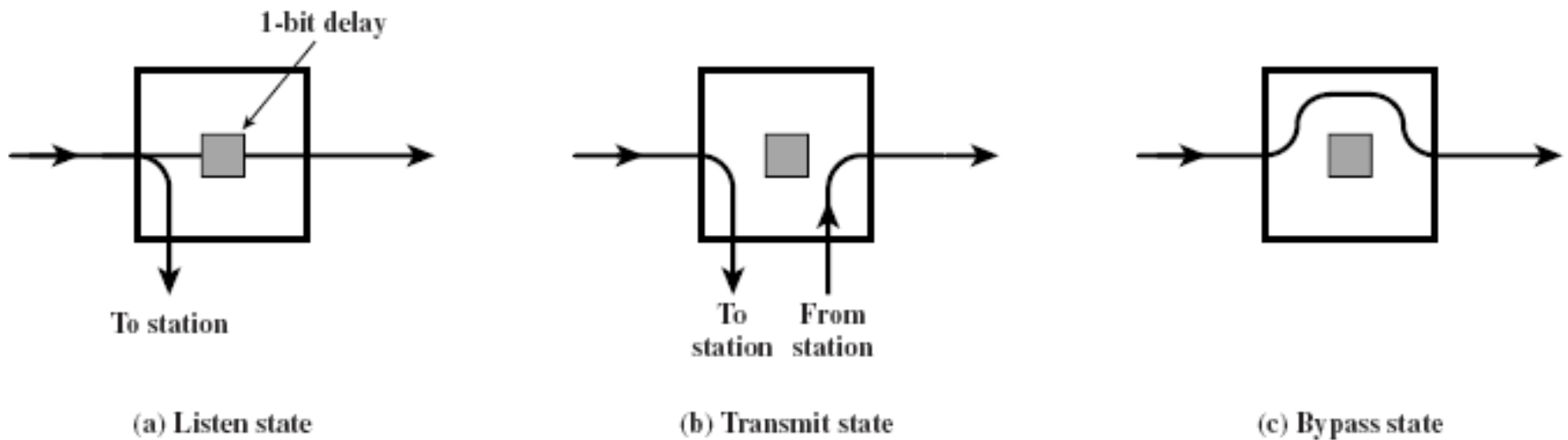


Figure 13.8 Ring Repeater States